A LOGIC MODULE USING TRANSFERRED-ELECTRON LOGIC DEVICES FOR TIME-OF-ARRIVAL DETERMINATION OF GHz SIGNALS*

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ABSTRACT

An experimental logic module for high precision time interval measurements is described. The fast switching properties of transferred-electron devices, MESFETs and SRDs are utilized in novel circuit designs for subnanosecond, single event measurements.

Introduction

The objective of this program is to develop an ultra-high-speed logic module which can be used to measure the time-difference-of-arrival (TDOA) of an rf signal at different parts of an antenna array. The logic module employs a vernier time-measurement scheme and utilizes the ultra-fast switching properties of transferred-electron logic devices (TELDs). Using this technique, it is possible to measure time intervals for nonperiodic and asynchronous waveforms. This method permits at least an order of magnitude reduction in clock frequency as was demonstrated by R.G. Baron (1). For example, a resolution of 100 ps can be obtained using a 1-GHz clock whereas a clock frequency of 10 GHz is required if a gated cw clock and counter are used.

The function of the TDOA system is to accurately measure the time-difference-of-arrival of a single rf burst at two isotropic antennas so that the direction of the rf source may be determined. The major parts of the system are the rf module, which consists of matched amplifiers and limiters to increase the signal from the antennas to a level capable of triggering three-terminal TELDs (about 0-10 dBm), and the TELD logic module with threshold gates and a vernier counter capable of subnanosecond resolution. The two TELD threshold gates generate start and stop pulses whose time difference is measured by the vernier and coarse time measurement components. The logic module is frequency independent and can be used with rf modules covering different frequency ranges.

The Vernier Time Measurement Subsystem

Figure 1 shows the layout of the logic module. The module's design is based upon the technique of vernier time measurement using two signal processing channels. The arrival of an rf signal above a threshold value at the early channel initiates a pulse train to be sent to the coincidence circuit which is illustrated as the clock pulse train in Fig. 2. This pulse train has constant amplitude pulses of fixed width and period T_C. A second pulse train is generated by the vernier channel which is illustrated as the vernier pulse train of Fig. 2; however, the period for this group is T_V. If M clock pulses occur before the start of the vernier channel and N clock pulses have occurred at coincidence, then the total time difference at the start of each pulse train is $(M-1)T_C + (N-M)\cdot(T_C-T_V)$ and the resolution is T_C-T_V.

The Breadboard Logic Module

A breadboard of the logic module has been designed. The two input threshold gates and the coincidence circuit utilize TELDs and the pulse burst generators are constructed with GaAs MESFETs. Step recovery diodes have been used for pulse shaping at several points in the circuit. The counters are commercially available and of ECL type.

A three-terminal transferred-electron logic device is used to construct an extremely fast and sensitive threshold gate. The TELD is operated in the memory mode so that an output is obtained only when the input signal first exceeds a predetermined threshold value. Figure 3 shows the threshold gate circuit and Fig. 4 shows the sharp transfer characteristic obtained with this circuit.

The TELD in the coincidence circuit was also operated in the memory mode. For this application, a split-gate TELD is preferable since the input signals are well isolated. However, the coincidence circuit constructed with a split-gate device had too low a triggering sensitivity for the present application. Therefore, the breadboard logic module was constructed with a single gate TELD using resistive signal combining.

The step output of each threshold gate is shaped into a single pulse by means of a step recovery diode (SRD) circuit. Each single pulse is used to drive a pulse train generator (constructed with MESFETs and transmission line networks) which in turn produces the clock pulse train and the vernier pulse train illustrated in Fig. 2. The experimental clock and vernier waveforms are shown in Fig. 5. The coincidence circuit then resolves the coincidence of these two pulse trains.

The breadboard system was designed, constructed, and tested without the ECL counters. Figure 6 is a schematic drawing of the breadboard logic module and Fig. 7 is a photograph of the actual system. Four pulses were used for each pulse burst generator and $T_C \approx 1.2$ ns. This produced a measured resolution of about 400 ps. In tests the output of the coincidence circuit was observed as the time delay of the input rf signal (0.8 GHz) to one channel was varied. The range of measurement (with counters) is about 2 ns, which is adequate for the TDOA application.

100-ps resolution should be obtainable in future designs by using at least eleven pulses and a clock pulse period of 1 ns. The range of time measurements can also be increased significantly for other applications.

Acknowledgments

The transferred-electron devices utilized in this program have been designed and developed by L.C. Upadhyayula and fabricated by R. Smith. The experimental circuits were constructed by J.F. Wilhelm, J.E. Brown, P. R. Pelka, O.M. Gervasoni and N.S. Klein. The MESFET devices were made available by J.J. Napoleon.

Reference

1. R. G. Baron, "The Vernier Time Measurement Technique," Proc. IRE, 45, 21-30, January 1957.

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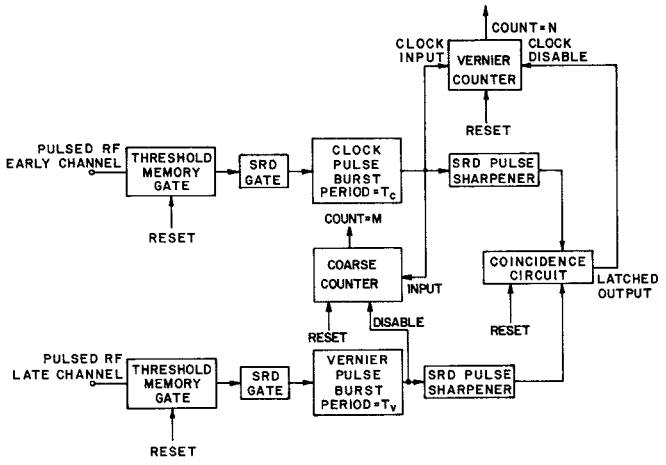

Figure 1. Logic module layout.

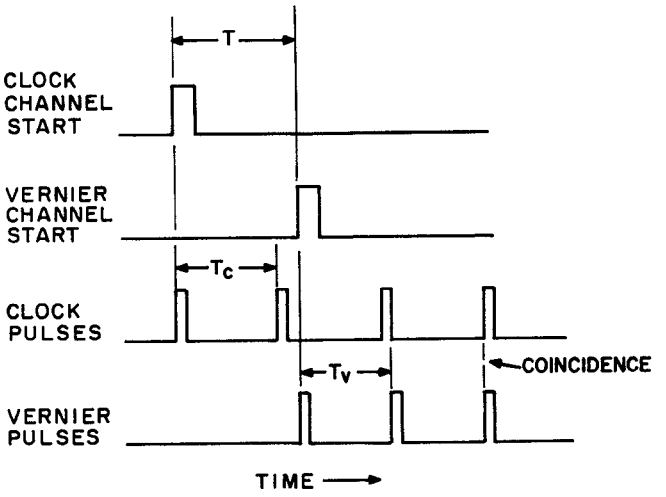

Figure 2. Pulse trains in vernier time measurement system.

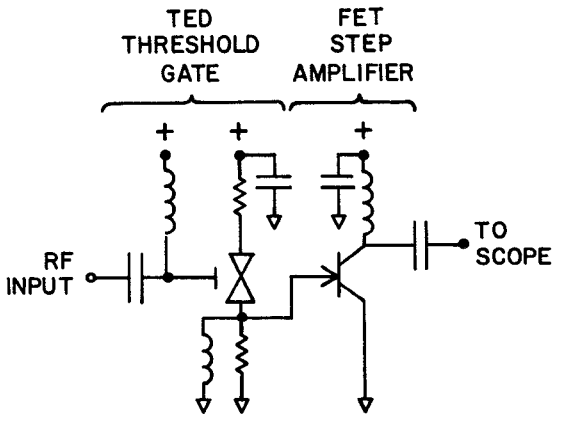

Figure 3. Threshold gate circuit.

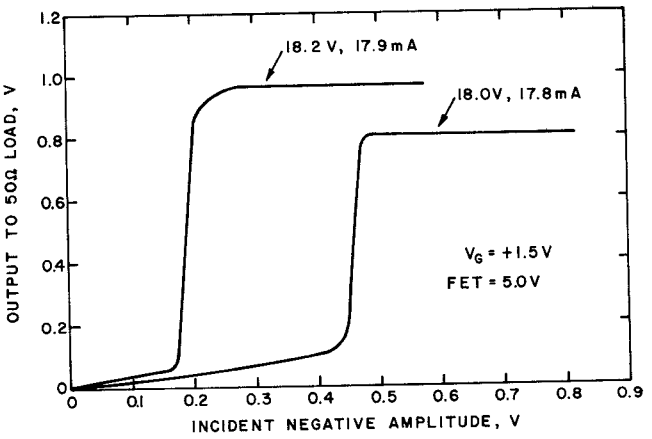

Figure 4. Threshold gate transfer characteristics with input rf burst at 800 MHz.

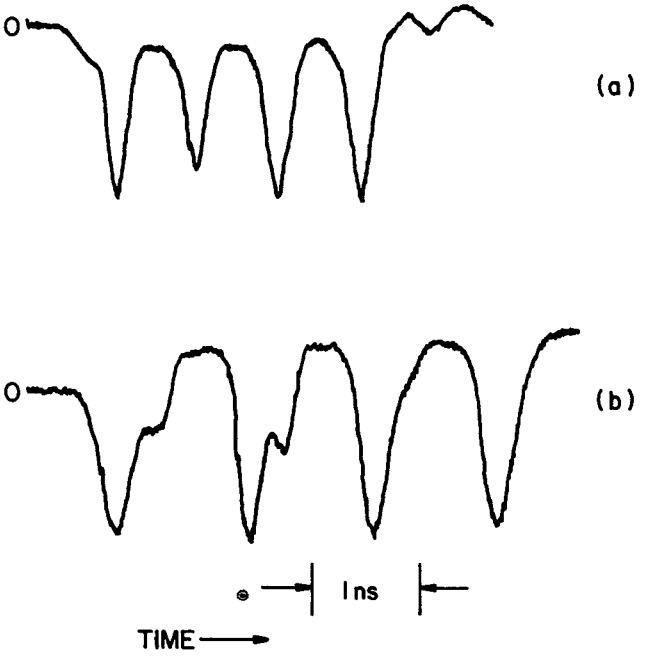

Figure 5. Experimental output waveform for (a) the vernier pulse burst generator and (b) the clock pulse burst generator.

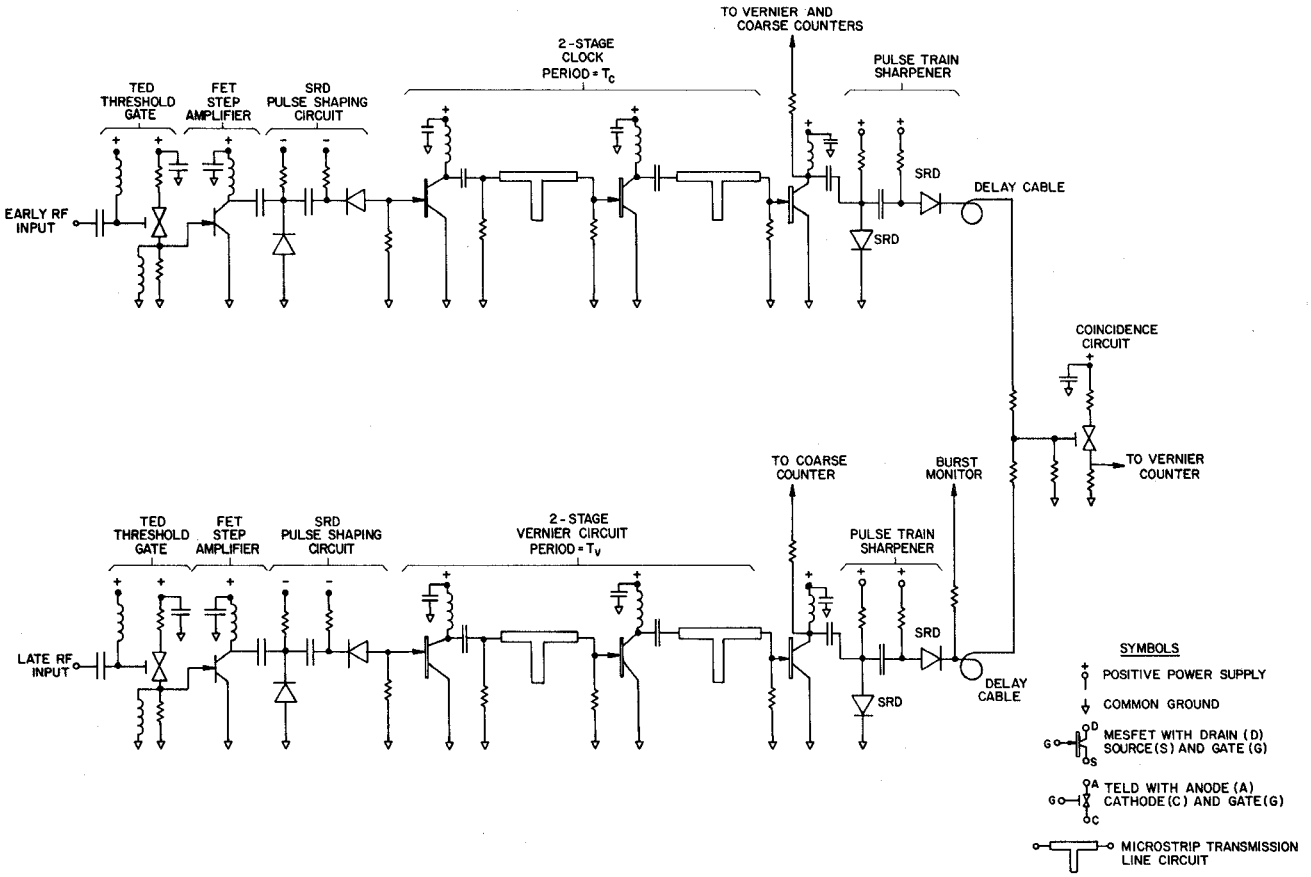

Figure 6. Breadboard logic module schematic.

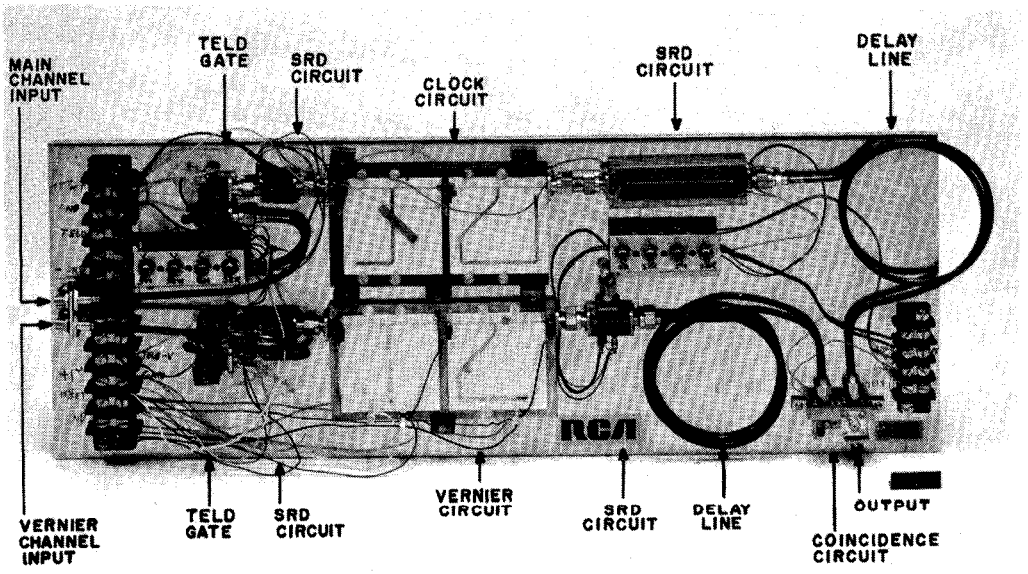

Figure 7. Photograph of breadboard logic module.